

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74AC161P, TC74AC161F, TC74AC161FN, TC74AC161FT
TC74AC163P, TC74AC163F, TC74AC163FN, TC74AC163FT

SYNCHRONOUS PRESETTABLE 4 – BIT BINARY COUNTER
TC74AC161P/F/FN/FT ASYNCHRONOUS CLEAR
TC74AC163P/F/FN/FT SYNCHRONOUS CLEAR

The TC74AC161 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate and double - layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLR}}$ inputs are active on low logic level.

Presetting of these IC's is synchronous to the rising edge of CK.

The clear function of the TC74AC163 is synchronous to CK, while the TC74AC161 are cleared asynchronously.

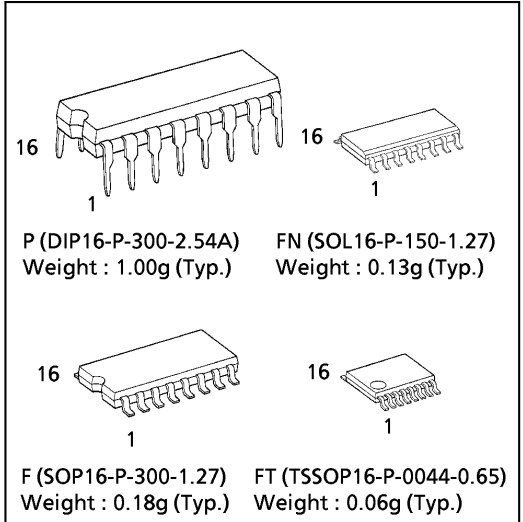
Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n - bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

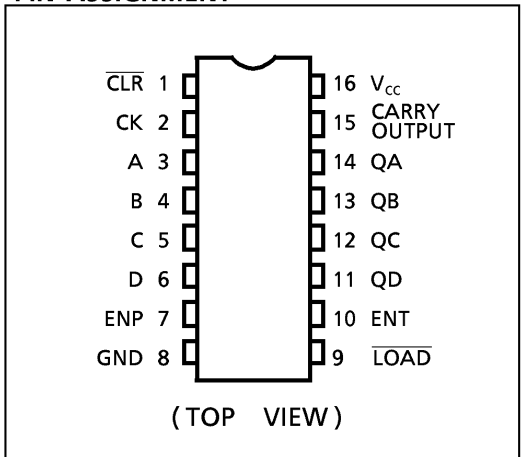
FEATURES:

- High Speed..... $f_{\text{MAX}} = 170\text{MHz}(\text{typ.})$ at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} (\text{Min.})$
- Symmetrical Output Impedance... $|I_{\text{OH}}| = |I_{\text{OL}}| = 24\text{mA}(\text{Min.})$
 Capability of driving 50 Ω transmission lines.
- Balanced Propagation Delays..... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F161/163

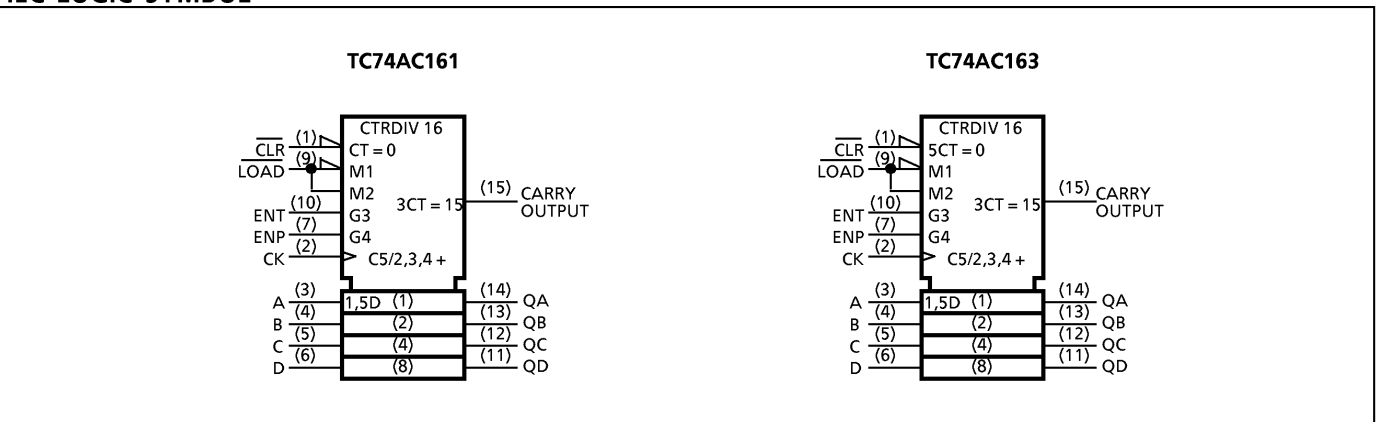
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



IEC LOGIC SYMBOL

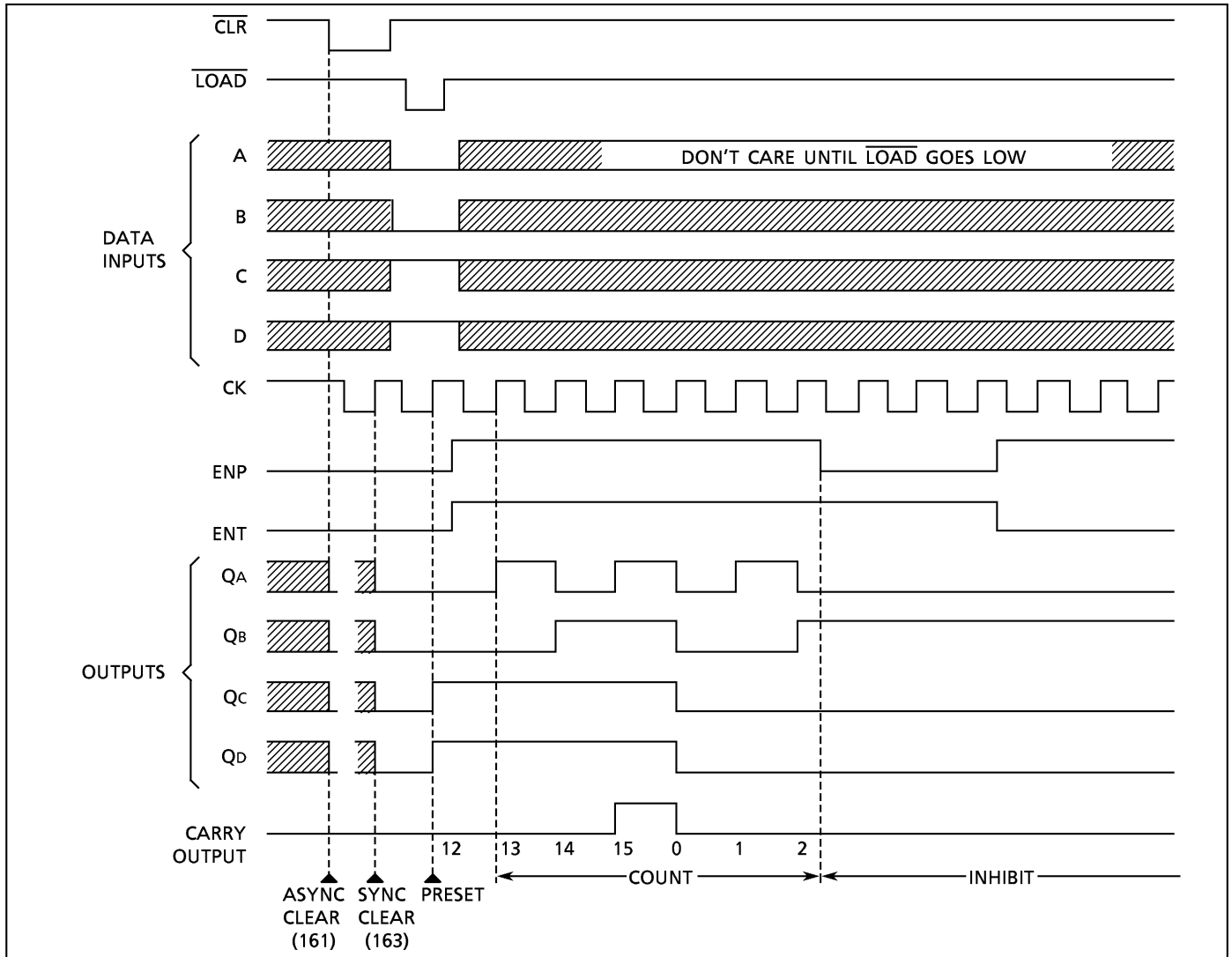


TRUTH TABLE

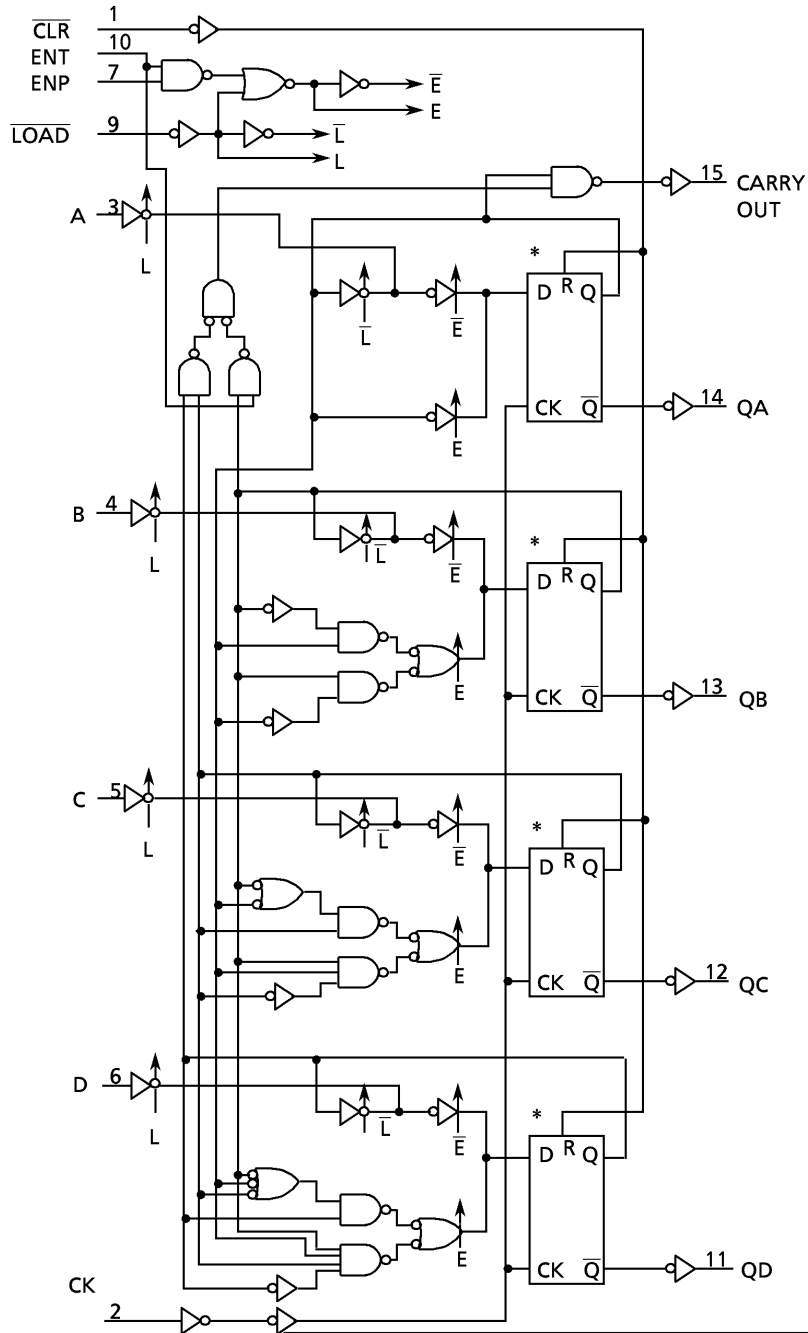
INPUTS							OUTPUTS				FUNCTION
CLR (161)	CLR (163)	LOAD	ENP	ENT	CK (161)	CK (163)	QA	QB	QC	QD	
L	L	X	X	X	X	\uparrow	L	L	L	L	RESET TO "0"
H	H	L	X	X	\uparrow	\uparrow	A	B	C	D	PRESET DATA
H	H	H	X	L	\uparrow	\uparrow	NO CHANGE				NO COUNT
H	H	H	L	X	\uparrow	\uparrow	NO CHANGE				NO COUNT
H	H	H	H	H	\uparrow	\uparrow	COUNT UP				COUNT
H	X	X	X	X	\downarrow	\downarrow	NO CHANGE				NO COUNT

Note X : Don't Care
 A, B, C, D : Logic Level of Data Inputs
 Carry : CARRY = ENT · QA · QB · QC · QD

TIMING CHART



SYSTEM DIAGRAM



* TRUTH TABLE OF INTERNAL F/F

TC74AC161					TC74AC163				
D	CK	R	Q	Q	D	CK	R	Q	Q̄
X	X	H	L	H	X	↑	H	L	H
L	↑	L	L	H	L	↑	L	L	H
H	↑	L	H	L	H	↑	L	H	L
X	↓	L	NO CHANGE		X	↓	L	NO CHANGE	

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±50	mA
DC Output Current	I _{OUT}	±50	mA
DC V _{CC} /Ground Current	I _{CC}	±125	mA
Power Dissipation	P _D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T _{stg}	-65~150	°C

*500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	2.0~5.5	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	dt/dV	0~100 (V _{CC} = 3.3 ± 0.3V) 0~20 (V _{CC} = 5 ± 0.5V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		2.0	1.50	—	—	1.50	—	V	
			3.0	2.10	—	—	2.10	—		
			5.5	3.85	—	—	3.85	—		
Low - Level Input Voltage	V _{IL}		2.0	—	—	0.50	—	0.50	V	
			3.0	—	—	0.90	—	0.90		
			5.5	—	—	1.65	—	1.65		
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0	1.9	2.0	—	1.9	V	
				3.0	2.9	3.0	—	2.9		—
				4.5	4.4	4.5	—	4.4		—
		3.0	I _{OH} = -4mA I _{OH} = -24mA I _{OH} = -75mA*	2.58	—	—	2.48	—		
				3.94	—	—	3.80	—		
				—	—	—	3.85	—		
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	—	0.0	0.1	—	V	
				3.0	—	0.0	0.1	—		0.1
				4.5	—	0.0	0.1	—		0.1
		3.0	I _{OL} = 12mA I _{OL} = 24mA I _{OL} = 75mA*	—	—	0.36	—	0.44		
				—	—	0.36	—	0.44		
				—	—	—	—	1.65		
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0		

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	Fig .1	3.3 ± 0.3	7.0	7.0	7.0	ns
			5.0 ± 0.5	5.0	5.0	5.0	
Minimum Pulse Width (\overline{CLR})*	$t_{W(L)}$	Fig .4	3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	7.0 5.0	
Minimum Set - up Time (\overline{LOAD} , ENP, ENT)	t_s	Fig .2, 3	3.3 ± 0.3 5.0 ± 0.5	11.0 7.0	13.0 7.0	13.0 7.0	
Minimum Set - up Time (A, B, C, D)	t_s	Fig .2	3.3 ± 0.3 5.0 ± 0.5	8.0 4.0	8.0 4.0	8.0 4.0	
Minimum Set - up Time (\overline{CLR})**	t_s	Fig .5	3.3 ± 0.3 5.0 ± 0.5	6.0 4.0	6.0 4.0	6.0 4.0	
Minimum Hold Time	t_h	Fig .2, 3, 5	3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	1.0 1.0	
Minimum Removal Time (\overline{CLR})*	t_{rem}	Fig .4	3.3 ± 0.3 5.0 ± 0.5	6.0 4.0	6.0 4.0	6.0 4.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500 Ω, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}	Fig.1	3.3 ± 0.3	—	8.8	15.8	1.0	18.0	ns
			5.0 ± 0.5	—	6.5	9.6	1.0	11.0	
Propagation Delay Time (CK-CARRY, Count Mode)	t_{pLH} t_{pHL}	Fig.1	3.3 ± 0.3	—	10.4	18.4	1.0	21.0	
			5.0 ± 0.5	—	8.1	11.8	1.0	13.5	
Propagation Delay Time (CK-CARRY, Preset Mode)	t_{pLH} t_{pHL}	Fig.2	3.3 ± 0.3	—	12.9	22.4	1.0	25.5	
			5.0 ± 0.5	—	9.1	13.2	1.0	15.0	
Propagation Delay Time (ENT-CARRY)	t_{pLH} t_{pHL}	Fig.6	3.3 ± 0.3	—	7.5	13.2	1.0	15.0	
			5.0 ± 0.5	—	5.8	8.3	1.0	9.5	
Propagation Delay Time (\overline{CLR} -Q)*	t_{pHL}	Fig.4	3.3 ± 0.3	—	10.6	18.4	1.0	21.0	
			5.0 ± 0.5	—	7.7	11.4	1.0	13.0	
Propagation Delay Time (\overline{CLR} -CARRY)*	t_{pHL}	Fig.4	3.3 ± 0.3	—	12.0	21.0	1.0	24.0	
			5.0 ± 0.5	—	8.6	12.7	1.0	14.5	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3 5.0 ± 0.5	50 90	110 140	— —	50 90	— —	MHz
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	85	—	—	—	

Note * for TC74AC161 only

** for TC74AC163 only

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

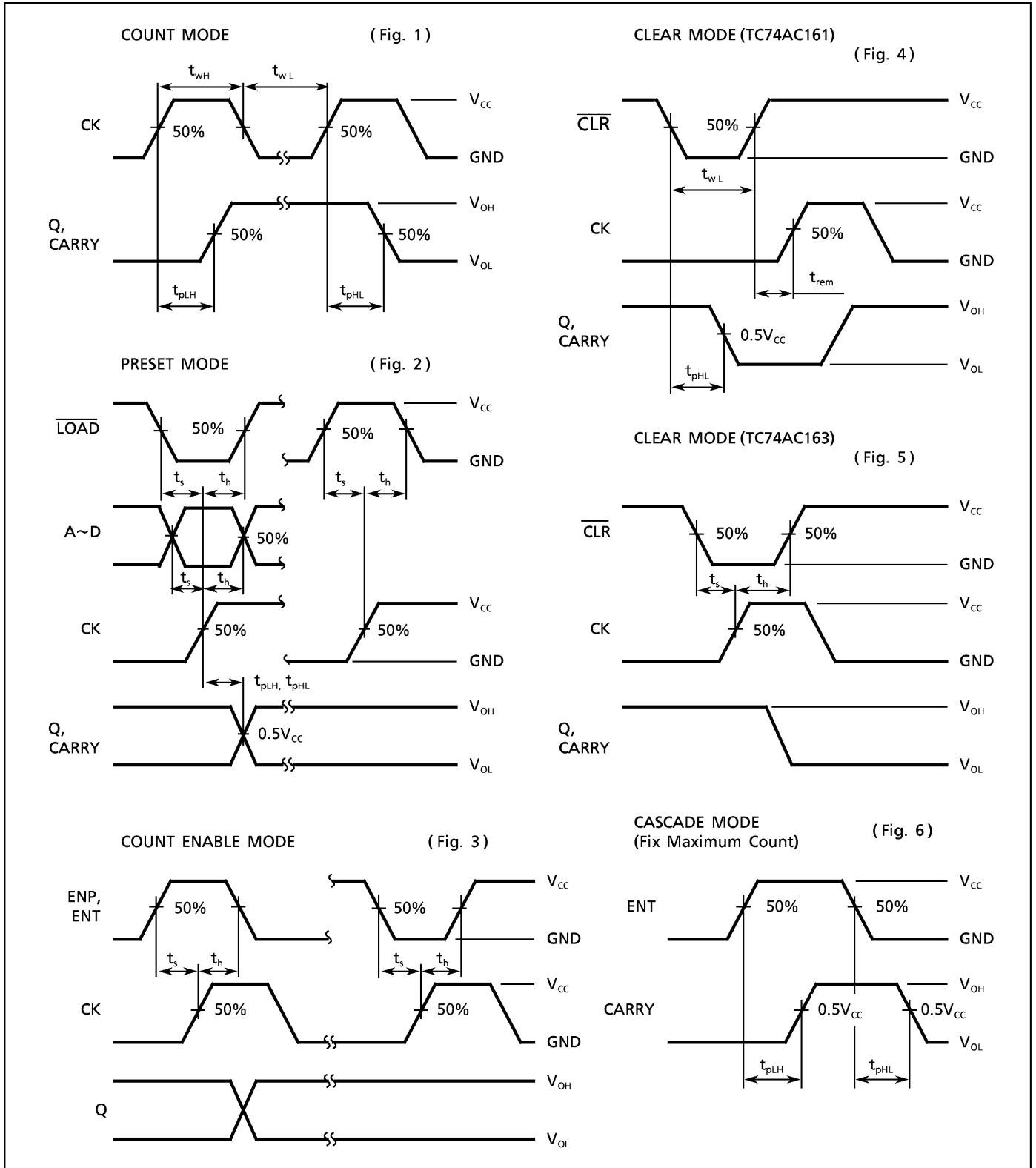
When the outputs drive a capacitive load, total current consumption is the sum of C_{PD} , and ΔI_{CC} which is obtained from the following formula :

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

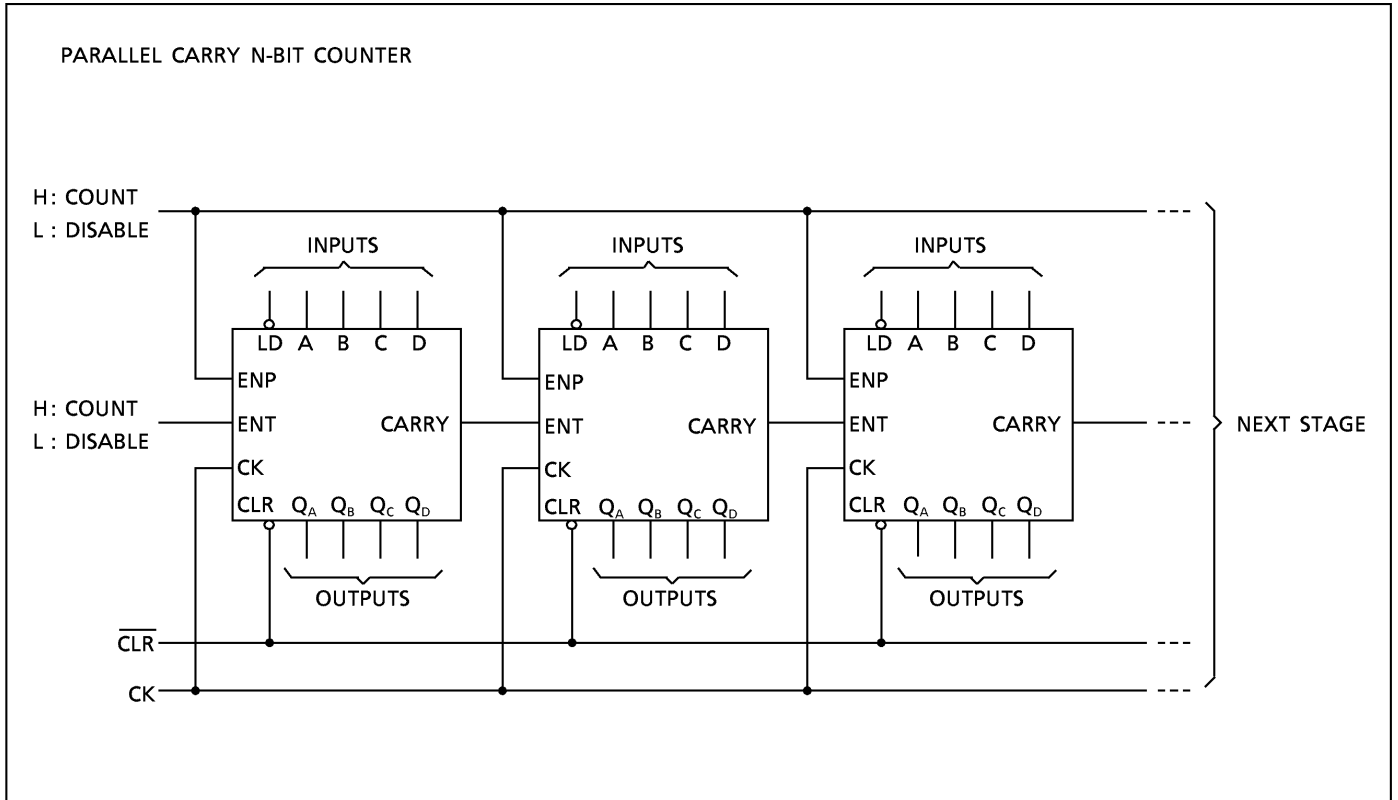
$C_{QA} \sim C_{QD}$ and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.

f_{CK} is the input frequency of the CK.

SWITCHING CHARACTERISTICS TEST WAVEFORM

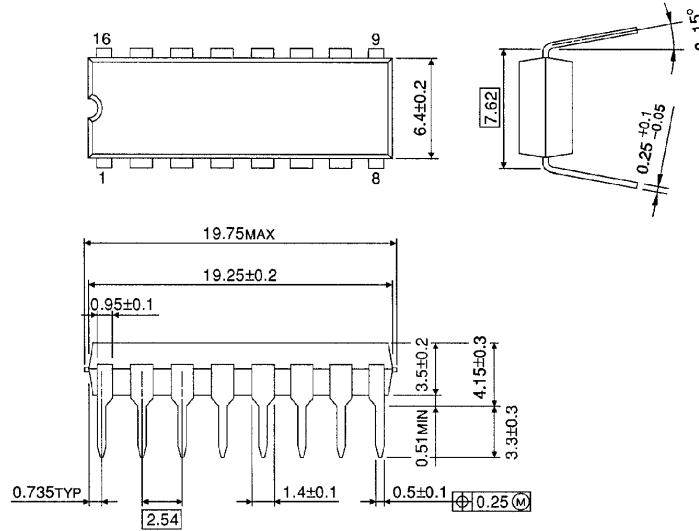


TYPICAL APPLICATION



DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

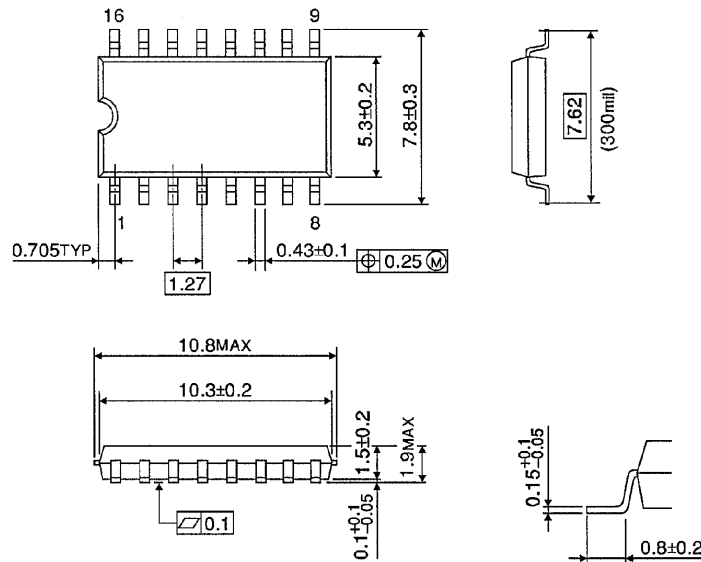
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

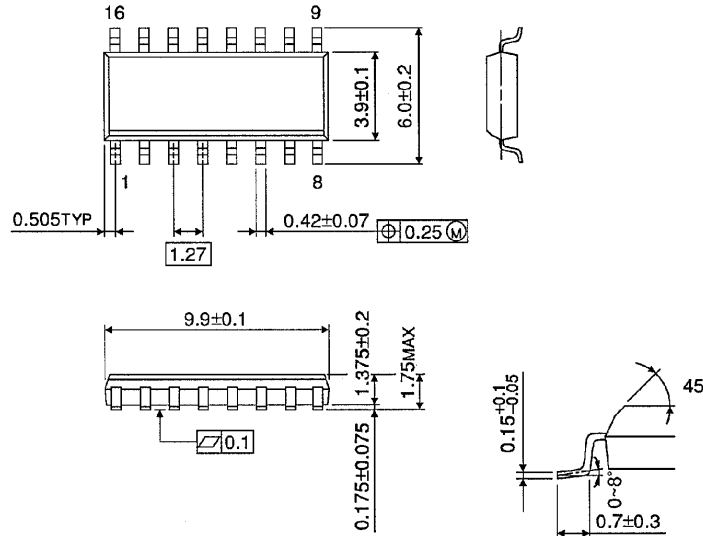


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

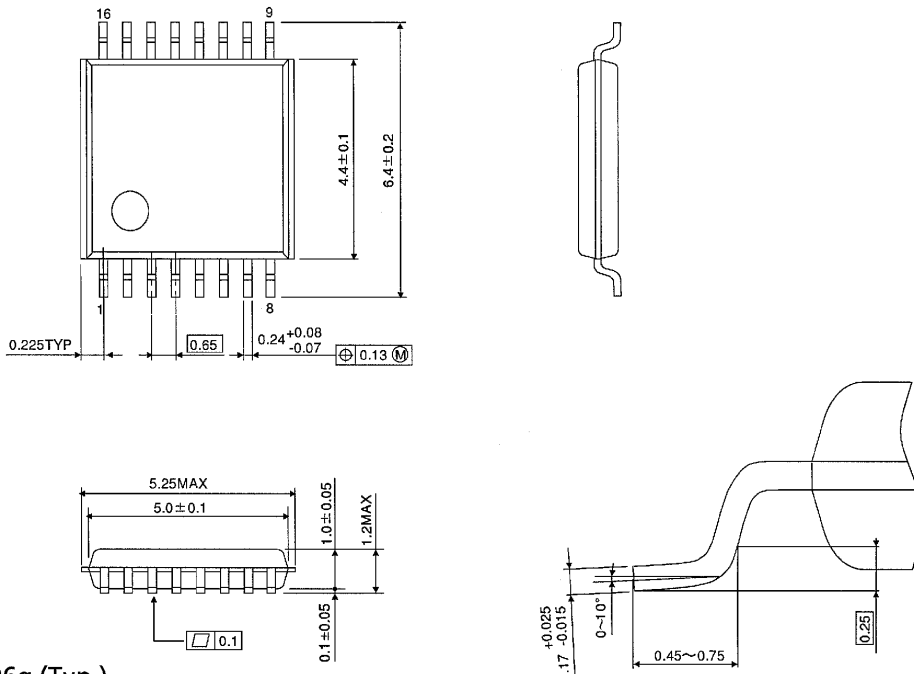
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)

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